Features

- **High-performance, High-density Programmable Logic Device**
  - **Typical 7 ns Pin-to-pin Delay**
  - **Fully Connected Logic Array with 416 Product Terms**
- **Flexible Output Macrocell**
  - **48 Flip-flops – Two per Macrocell**
  - **72 Sum Terms**
  - **All Flip-flops, I/O Pins Feed in Independently**
  - **Achieves Over 80% Gate Utilization**
- **Enhanced Macrocell Configuration Selections**
  - **D- or T-type Flip-flops**
  - **Product Term or Direct Input Pin Clocking**
  - **Registered or Combinatorial Internal Feedback**
- **Several Power Saving Options**

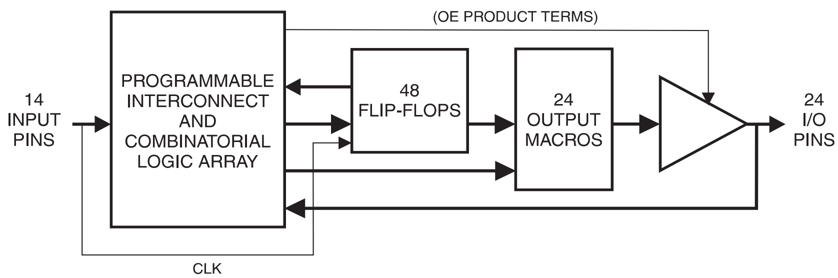
Device	I_{CC}, Standby
ATV2500B	110 mA
ATV2500BQ	30 mA
ATV2500BL	2 mA
ATV2500BQL	2 mA

- **Backward Compatible with ATV2500H/L Software**
- **Proven and Reliable High-speed UV EPROM Process**
- **Reprogrammable – Tested 100% for Programmability**
- **40-lead Dual-in-line and 44-lead Surface Mount Packages**

High-speed High-density UV-erasable Programmable Logic Device

ATV2500B ATV2500BQ ATV2500BQL

Block Diagram

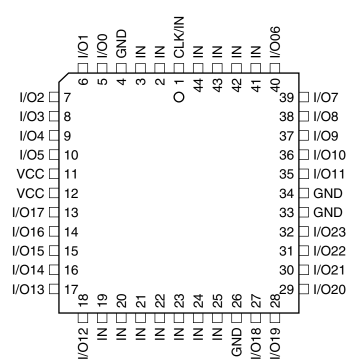


Pin Configurations

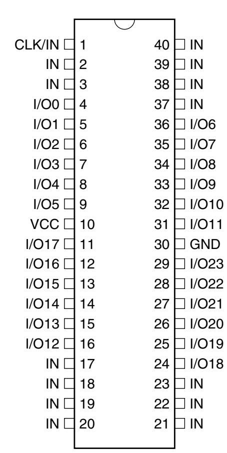
Pin Name	Function
IN	Logic Inputs
CLK/IN	Pin Clock and Input
I/O	Bi-directional Buffers
I/O 0,2,4..	“Even” I/O Buffers
I/O 1,3,5..	“Odd” I/O Buffers
GND	Ground
VCC	+5V Supply

Note: For ATV2500BQ and ATV2500BQL (PLCC/LCC package only) pin 4 and pin 26 connections are not required.

LCC/PLCC

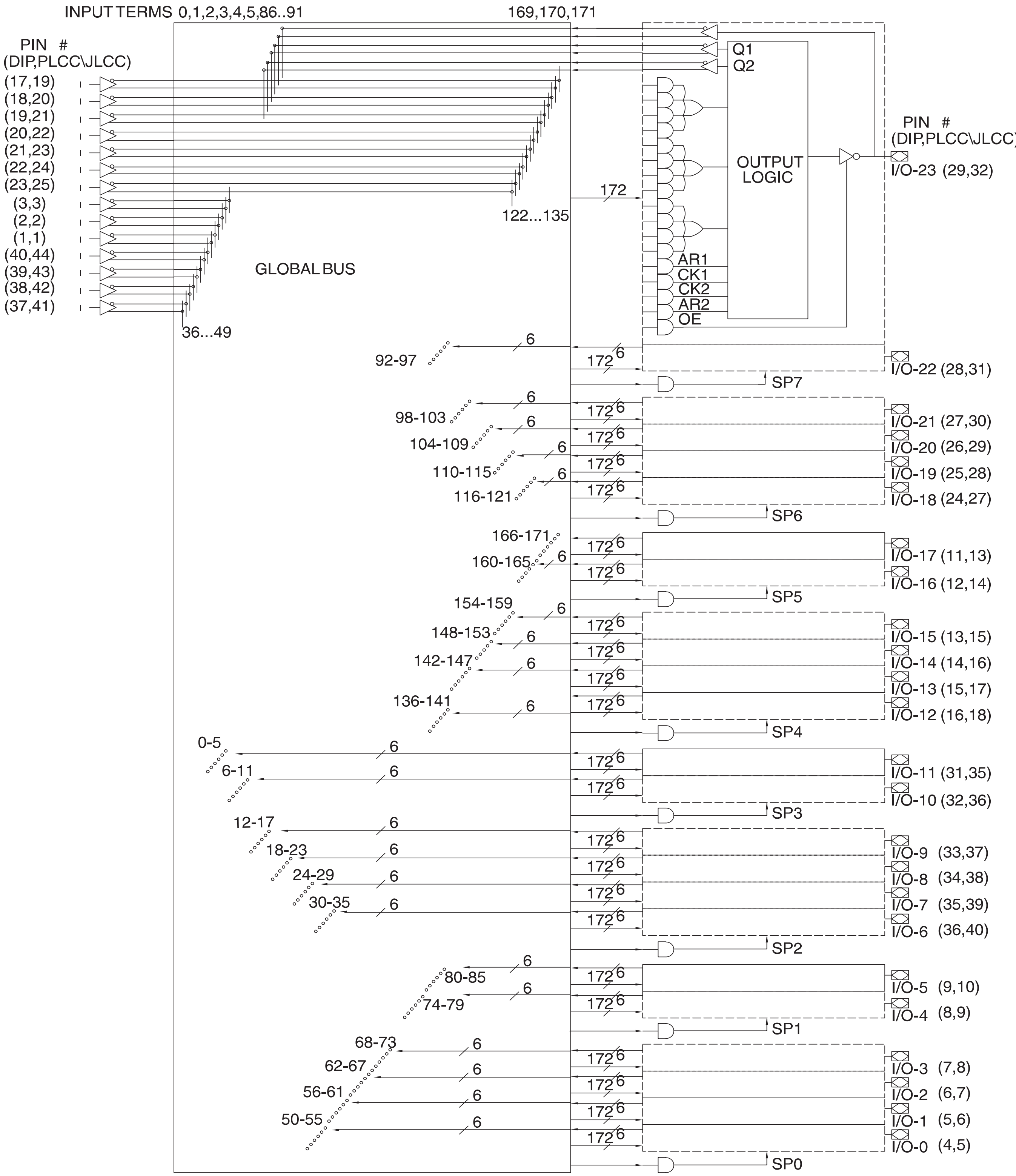


DIP



Rev. 0249J–05/00

Functional Logic Diagram ATV2500B



Note: 1. Not required for PLCC versions of ATV2500BQ or ATV2500BQL, making them compatible with ATV2500H and ATV2500L pinout.

Description

The ATV2500Bs are the highest density PLDs available in a 40- or 44-lead package. With their fully connected logic array and flexible macrocell structure, high-gate utilization is easily obtainable.

The ATV2500Bs are organized around a *single universal and-or array.* All pins and feedback terms are always available to every macrocell. Each of the 38 logic pins are array inputs, as are the outputs of each flip-flop.

In the ATV2500Bs, four product terms are input to each sum term. Furthermore, each macrocell's three sum terms can be combined to provide up to 12 product terms per sum term with *no performance penalty.* Each flip-flop is individually selectable to be either D- or T-type, providing further logic compaction. Also, 24 of the flip-flops may be bypassed to provide internal combinatorial feedback to the logic array.

Product terms provide individual clocks and asynchronous resets for each flip-flop. The flip-flops may also be individually configured to have direct input pin clocking. Each output has its own enable product term. Eight synchronous preset product terms serve local groups of either four or eight flip-flops. Register preload functions are provided to simplify testing. All registers automatically reset upon power-up.

Several low-power device options allow selection of the optimum solution for many power-sensitive applications. Each of the options significantly reduces total system power and enhances system reliability.

Functional Logic Diagram Description

The ATV2500B functional logic diagram describes the interconnections between the input, feedback pins and logic cells. All interconnections are routed through the single global bus.

The ATV2500Bs are straightforward and uniform PLDs. The 24 macrocells are numbered 0 through 23. Each macrocell contains 17 AND gates. All AND gates have 172 inputs. The five lower product terms provide AR1, CK1, CK2, AR2, and OE. These are: one asynchronous reset and clock per flip-flop, and an output enable. The top 12 product terms are grouped into three sum terms, which are used as shown in the macrocell diagrams.

Eight synchronous preset terms are distributed in a 2/4 pattern. The first four macrocells share Preset 0, the next two share Preset 1, and so on, ending with the last two macrocells sharing Preset 7.

The 14 dedicated inputs and their complements use the numbered positions in the global bus as shown. Each macrocell provides six inputs to the global bus: (left to right) feedback F2[1] true and false, flip-flop Q1 true and false, and the pin true and false. The positions occupied by these signals in the global bus are the six numbers in the bus diagram next to each macrocell.

Note: 1. Either the flip-flop input (D/T2) or output (Q2) may be

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V(1)
Voltage on Input Pins with Respect to Ground During Programming	-2.0V to +14.0V(1)
Programming Voltage with Respect to Ground	-2.0V to +14.0V(1)
Integrated UV Erase Dose	7258 W•sec/cm^2

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V DC which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} + 0.75V DC which may overshoot to +7.0V for pulses of less than 20 ns.

DC and AC Operating Conditions

	Commercial	Industrial	Military
Operating Temperature	0°C - 70°C (Ambient)	-40°C - 85°C (Ambient)	-55°C - 125°C (Case)
V_{CC} Power Supply	5V ± 5%	5V ± 10%	5V ± 10%

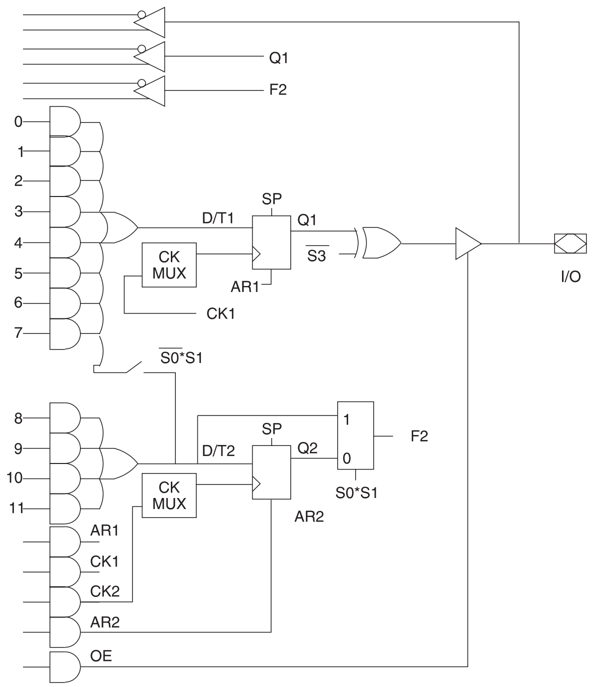
Pin Capacitance

f = 1 MHz, T = 25°C(1)

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Output Logic, Registered[1]



S2 = 0		Terms in		
S1	S0	D/T1	D/T2	Output Configuration
0	0	8	4	Registered (Q1); Q2 FB
1	0	12	4[1]	Registered (Q1); Q2 FB
1	1	8	4	Registered (Q1); D/T2 FB

S3	Output Configuration
0	Active Low
1	Active High

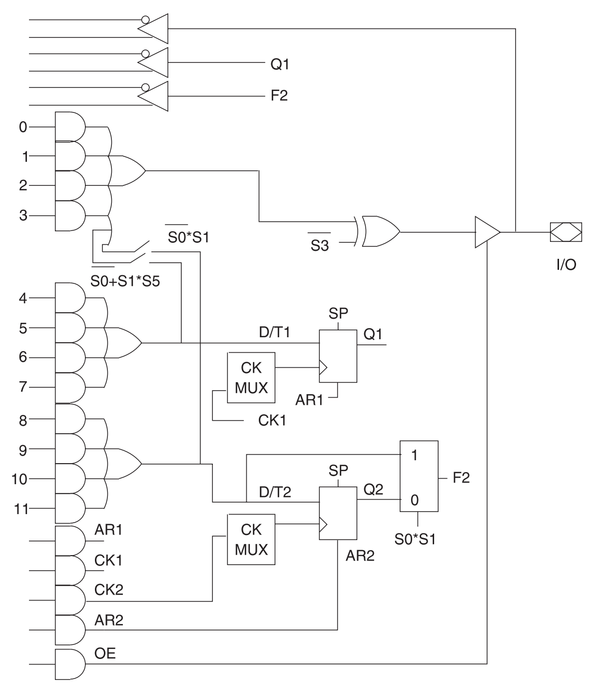
S6	Q1 CLOCK
0	CK1
1	CK1 • PIN1

S4	Register 1 Type
0	D
1	T

S7	Q2 CLOCK
0	CK2
1	CK2 • PIN1

S5	Register 2 Type
0	D
1	T

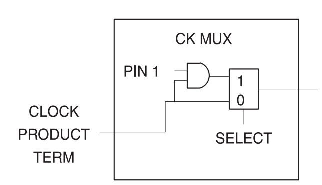
Output Logic, Combinatiorial[1]



S2 = 1			Terms in		
S5	S1	S0	D/T1	D/T2	Output Configuration
X	0	0	4[1]	4	Combinatorial (8 Terms); Q2 FB
X	0	1	4	4	Combinatorial (4 Terms); Q2 FB
X	1	0	4[1]	4[1]	Combinatorial (12 Terms); Q2 FB
1	1	1	4[1]	4	Combinatorial (8 Terms); D/T2 FB
0	1	1	4	4	Combinatorial (4 Terms); D/T2 FB

Note: 1. These four terms are shared with D/T1.

Clock Option



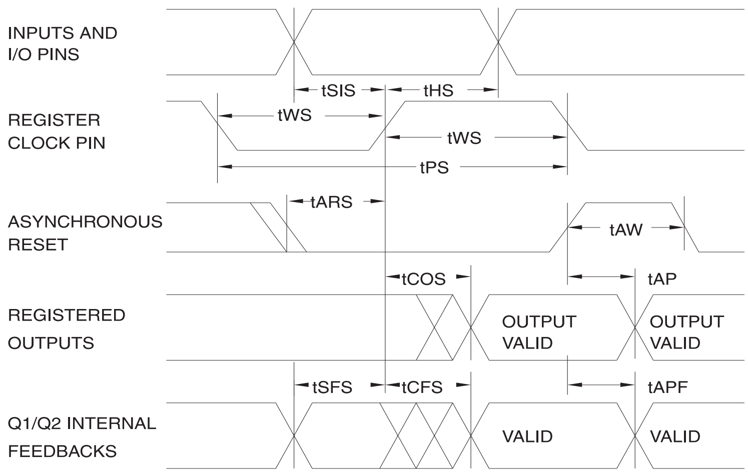
Note: 1. These diagrams show equivalent logic functions, not necessarily the actual circuit implementation.

DC Characteristics

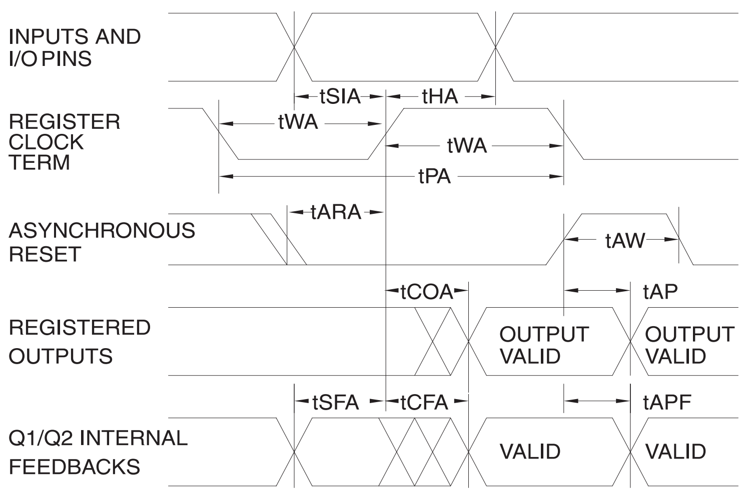
<table>
<tr><th>Symbol</th><th>Parameter</th><th colspan="3">Condition</th><th>Min</th><th>Typ</th><th>Max</th><th>Units</th></tr>
<tr><td>I_{IL}</td><td>Input Load Current</td><td colspan="3">V_{IN} = -0.1V to V_{CC} + 1V</td><td></td><td></td><td>10</td><td>µA</td></tr>
<tr><td>I_{LO}</td><td>Output Leakage Current</td><td colspan="3">V_{OUT} = -0.1V to V_{CC} + 0.1V</td><td></td><td></td><td>10</td><td>µA</td></tr>
<tr><td rowspan="8">I_{CC}</td><td rowspan="8">Power Supply Current, Standby</td><td rowspan="8">V_{CC} = MAX,
V_{IN} = GND or
V_{CC} f = 0 MHz,
Outputs Open</td><td rowspan="2">ATV2500B</td><td>Com.</td><td></td><td>110</td><td>190</td><td>mA</td></tr>
<tr><td>Ind., Mil.</td><td></td><td>110</td><td>210</td><td>mA</td></tr>
<tr><td rowspan="2">ATV2500BQ</td><td>Com.</td><td></td><td>30</td><td>70</td><td>mA</td></tr>
<tr><td>Ind., Mil.</td><td></td><td>30</td><td>85</td><td>mA</td></tr>
<tr><td rowspan="2">ATV2500BL</td><td>Com.</td><td></td><td>2</td><td>5</td><td>mA</td></tr>
<tr><td>Ind., Mil.</td><td></td><td>2</td><td>10</td><td>mA</td></tr>
<tr><td rowspan="2">ATV2500BQL</td><td>Com.</td><td></td><td>2</td><td>4</td><td>mA</td></tr>
<tr><td>Ind., Mil.</td><td></td><td>2</td><td>5</td><td>mA</td></tr>
<tr><td>I_{OS}</td><td>Output Short Circuit Current</td><td colspan="3">V_{OUT} = 0.5V</td><td></td><td></td><td>-120</td><td>mA</td></tr>
<tr><td>V_{IL}</td><td>Input Low Voltage</td><td colspan="3">MIN ≤ V_{CC} ≤ MAX</td><td>-0.6</td><td></td><td>0.8</td><td>V</td></tr>
<tr><td>V_{IH}</td><td>Input High Voltage</td><td colspan="3"></td><td>2.0</td><td></td><td>V_{CC} + 0.75</td><td>V</td></tr>
<tr><td rowspan="2">V_{OL}</td><td rowspan="2">Output Low Voltage</td><td rowspan="2">V_{IN} = V_{IH} or V_{IL},
V_{CC} = 4.5V</td><td>I_{OL} = 8 mA</td><td>Com., Ind.</td><td></td><td></td><td>0.5</td><td>V</td></tr>
<tr><td>I_{OL} = 6 mA</td><td>Mil.</td><td></td><td></td><td>0.5</td><td>V</td></tr>
<tr><td rowspan="2">V_{OH}</td><td rowspan="2">Output High Voltage</td><td rowspan="2">V_{CC} = MIN</td><td colspan="2">I_{OH} = -100 µA</td><td>V_{CC} - 0.3</td><td></td><td></td><td>V</td></tr>
<tr><td colspan="2">I_{OH} = -4.0 mA</td><td>2.4</td><td></td><td></td><td></td></tr>
</table>

Note: 1. See I_{CC} versus frequency characterization curves.

AC Waveforms(1) Input Pin Clock



AC Waveforms(1) Product Term Clock



Note: 1. Timing measurement reference is 1.5V. Input AC driving levels are 0.0V and 3.0V, unless otherwise specified.

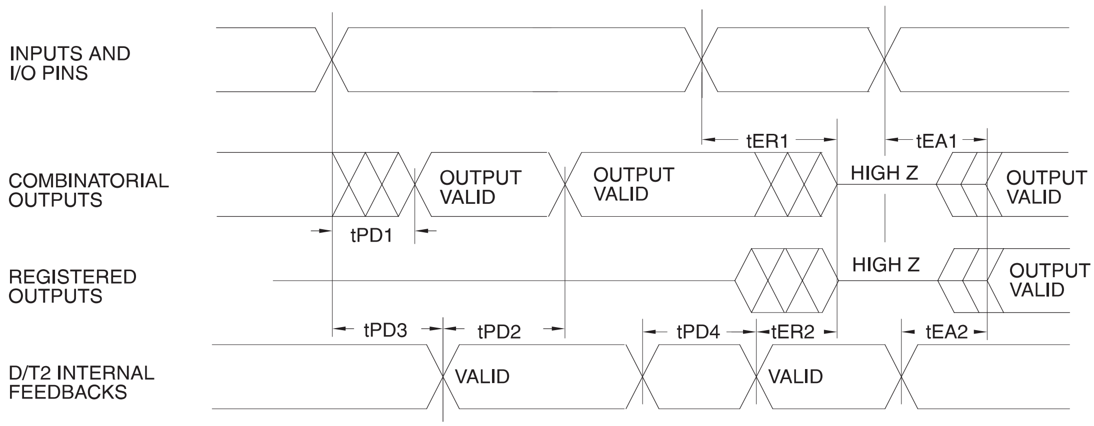
Register AC Characteristics, Input Pin Clock

Symbol	Parameter	-12		-15		-20		-25		-30		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{COS}	Clock to Output		7.5		10		11		12		15	ns
t_{CFS}	Clock to Feedback	0	4	0	5	0	6	0	7	0	8	ns
t_{SIS}	Input Setup Time	7		9		14		20		23		ns
t_{SFS}	Feedback Setup Time	7		9		14		20		23		ns
t_{HS}	Hold Time	0		0		0		0		0		ns
t_{WS}	Clock Width	5		6		7		8		9		ns
t_{PS}	Clock Period	10		12		14		16		18		ns
F_{MAXS}	External Feedback $1/(t_{SIS} + t_{COS})$		69		52		40		31		26	MHz
	Internal Feedback $1/(t_{SFS} + t_{CFS})$		90		71		50		37		32	MHz
	No Feedback $1/(t_{PS})$		100		83		71		62		55	MHz
t_{ARS}	Asynchronous Reset/Preset Recovery Time	7		12		15		20		25		ns

Register AC Characteristics, Product Term Clock

Symbol	Parameter	-12		-15		-20		-25		-30		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{COA}	Clock to Output		12		15		20		22		25	ns
t_{CFA}	Clock to Feedback	3	7	5	12	10	16	12	18	13	20	ns
t_{SIA}	Input Setup Time	4		5		10		15		19		ns
t_{SFA}	Feedback Setup Time	4		5		8		10		10		ns
t_{HA}	Hold Time	3		5		10		12		13		ns
t_{WA}	Clock Width	5.5		7.5		11		14		15		ns
t_{PA}	Clock Period	11		15		22		28		30		ns
F_{MAXA}	External Feedback $1/(t_{SIA} + t_{COA})$		62.5		50		33		27		23	MHz
	Internal Feedback $1/(t_{SFA} + t_{CFA})$		90		58		38		36		24	MHz
	No Feedback $1/(t_{PS})$		90		66		45		36		33	MHz
t_{ARA}	Asynchronous Reset/Preset Recovery Time	3		8		12		15		18		ns

AC Waveforms[1] Combinatorial Outputs and Feedback

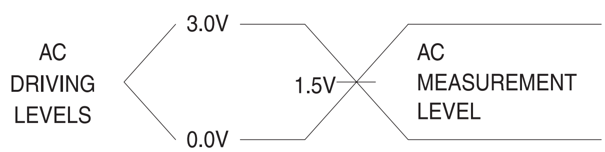


Note: 1. Timing measurement reference is 1.5V. Input AC driving levels are 0.0V and 3.0V, unless otherwise specified.

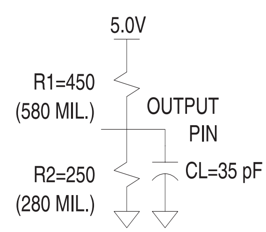
AC Characteristics

Symbol	Parameter	-12		-15		-20		-25		-30		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD1}	Input to Non-registered Output		12		15		20		25		30	ns
t_{PD2}	Feedback to Non-registered Output		12		15		20		25		30	ns
t_{PD3}	Input to Non-registered Feedback		8		11		15		18		20	ns
t_{PD4}	Feedback to Non-registered Feedback		8		11		15		18		20	ns
t_{EA1}	Input to Output Enable		12		15		20		25		30	ns
t_{ER1}	Input to Output Disable		12		15		20		25		30	ns
t_{EA2}	Feedback to Output Enable		12		15		20		25		30	ns
t_{ER2}	Feedback to Output Disable		12		15		20		25		30	ns
t_{AW}	Asynchronous Reset Width	6		8		12		15		18		ns
t_{AP}	Asynchronous Reset to Registered Output		15		18		22		28		30	ns
t_{APF}	Asynchronous Reset to Registered Feedback		12		15		19		25		30	ns

Input Test Waveforms and Measurement Levels



Output Test Load

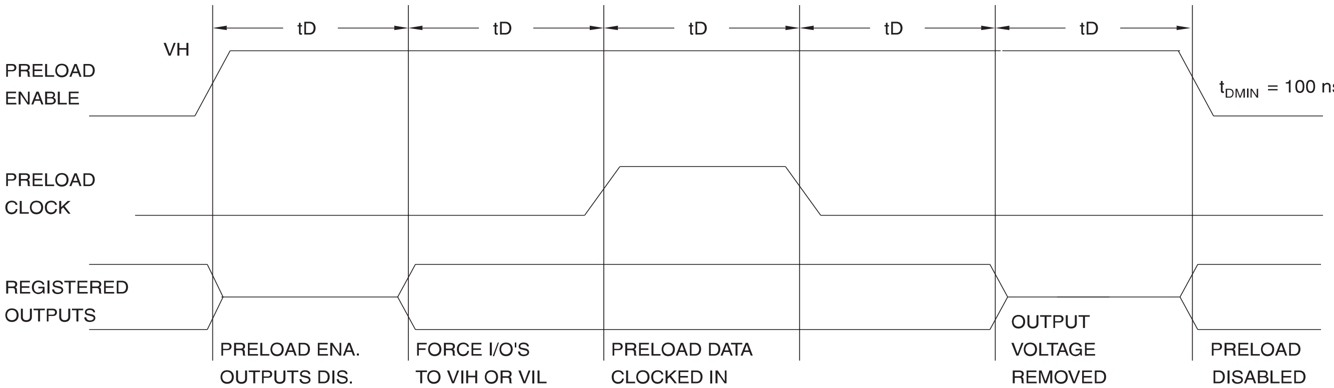


Preload and Observability of Registered Outputs

The ATV2500Bs registers are provided with circuitry to allow loading of each register asynchronously with either a high or a low. This feature will simplify testing since any state can be forced into the registers to control test sequencing. A V_{IH} level on the odd I/O pins will force the appropriate register high; a V_{IL} will force it low, independent of the polarity or other configuration bit settings.

The PRELOAD state is entered by placing an 10.25V to 10.75V signal on SMP lead 42. When the preload clock SMP lead 23 is pulsed high, the data on the I/O pins is placed into the 12 registers chosen by the Q select and even/odd select pins.

Register 2 observability mode is entered by placing an 10.25V to 10.75V signal on pin/lead 2. In this mode, the contents of the buried register bank will appear on the associated outputs when the OE control signals are active.



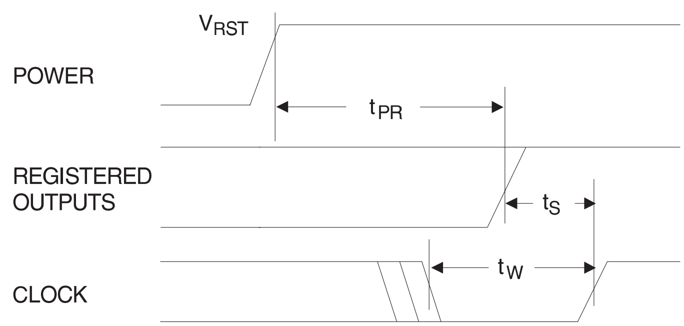
Level Forced on Odd I/O Pin during PRELOAD Cycle	Q Select Pin State	Even/Odd Select	Even Q1 State after Cycle	Even Q2 State after Cycle	Odd Q1 State after Cycle	Odd Q2 State after Cycle
V_{IH}/V_{IL}	Low	Low	High/Low	X	X	X
V_{IH}/V_{IL}	High	Low	X	High/Low	X	X
V_{IH}/V_{IL}	Low	High	X	X	High/Low	X
V_{IH}/V_{IL}	High	High	X	X	X	High/Low

Power-up Reset

The registers in the ATV2500Bs are designed to reset during power-up. At a point delayed slightly from V_{CC} crossing V_{RST}, all registers will be reset to the low state. The output state will depend on the polarity of the output buffer.

This feature is critical for state as nature of reset and the uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

1. The V_{CC} rise must be monotonic,
2. After reset occurs, all input and feedback setup times must be met before driving the clock pin or terms high, and
3. The clock pin, and any signals from which clock terms are derived, must remain stable during t_{PR}.



Parameter	Description	Typ	Max	Units
t_{PR}	Power-up Reset Time	600	1000	ns
V_{RST}	Power-up Reset Voltage	3.8	4.5	V

Security Fuse Usage

A single fuse is provided to prevent unauthorized copying of ATV2500B fuse patterns. Once programmed, the outputs will read programmed during verify. The security fuse should be programmed last, as its effect is immediate.

The security fuse also inhibits Preload and Q2 observability.

Atmel CMOS PLDs

The ATV2500Bs utilize an advanced 0.65-micron CMOS EPROM technology. This technology's state of the art features are the optimum combination for PLDs:

- CMOS technology provides high speed, low power, and high noise immunity.
- EPROM technology is the most cost effective method for producing PLDs – surpassing bipolar fusible link technology in low cost, while providing the necessary reprogrammability.
- EPROM reprogrammability, which is 100% tested before shipment, provides inherently better programmability and reliability than one-time fusible PLDs.

Using the ATV2500Bs Many Advanced Features

The ATV2500Bs advanced flexibility packs more usable gates into 44 leads than other PLDs. Some of the ATV2500Bs key features are:

- **Fully Connected Logic Array –** Each array input is always available to every product term. This makes logic placement a breeze.
- **Selectable D- and T-Type Registers –** Each ATV2500B flip-flop can be individually configured as either D- or T-type. Using the T-type configuration, JK and SR flip-flops are also easily created. These options allow more efficient product term usage.
- **Buried Combinatorial Feedback –** Each macrocell's Q2 register may be bypassed to feed its input (D/T2) directly back to the logic array. This provides further logic expansion capability without using precious pin resources.
- **Selectable Synchronous/Asynchronous Clocking –** Each of the ATV2500Bs flip-flops has a dedicated clock product term. This removes the constraint that all registers use the same clock. Buried state machines, counters and registers can all coexist in one device while running on separate clocks. Individual flip-flop clock source selection further allows mixing higher performance pin clocking and flexible product term clocking within one design.
- **A Total of 48 Registers –** The ATV2500B provides two flip-flops per macrocell – a total of 48. Each register has its own clock and reset terms, as well as its own sum term.
- **Independent I/O Pin and Feedback Paths –** Each I/O pin on the ATV2500B has a dedicated input path. Each of the 48 registers has its own feedback term into the array as well. These features, combined with individual product terms for each I/O's output enable, facilitate true bi-directional I/O design.
- **Combinable Sum Terms –** Each output macrocell's three sum terms may be combined into a single term. This provides a fan in of up to 12 product terms per sum term with *no speed penalty.*

Programming Software Support

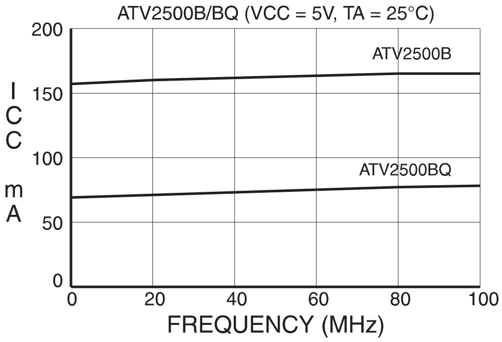
As with all other Atmel PLDs, several third party PLD development software products and programmers will support the ATV2500Bs.

Several third party programmers will support the ATV2500B as well. Additionally, the ATV2500B may be programmed to perform the ATV2500H/Ls functional subset (no T-type flip-flops, pin clocking or D/T2 feedback) using the ATV2500H/L JEDEC file. In this case, the ATV2500B becomes a direct replacement or speed upgrade for the ATV2500H/L (additional GND connections are required). Please refer to the Programmable Logic Development Tools section for a complete PLD software and programmer listing.

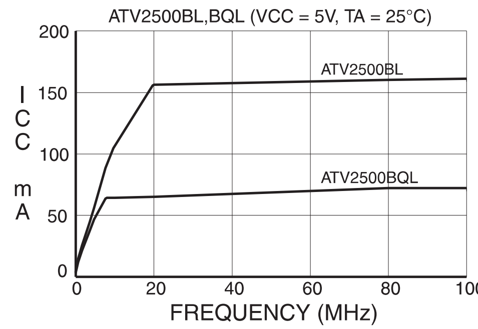
Erasure Characteristics

The entire memory array of an ATV2500B is erased after exposure to ultraviolet light at a wavelength of 2537 Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 $\mu W/cm^2$ intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of 15 $W \cdot sec/cm^2$. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable PLD which will be subjected to continuous fluorescent indoor lighting or sunlight.

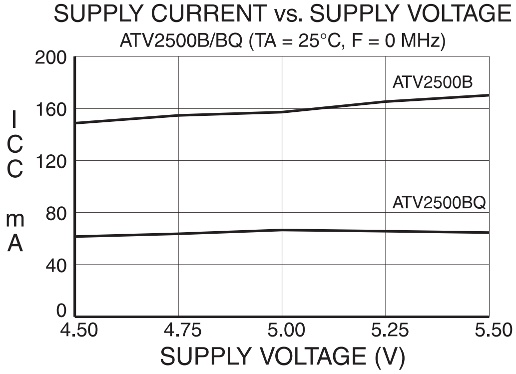
SUPPLY CURRENT vs. INPUT FREQUENCY



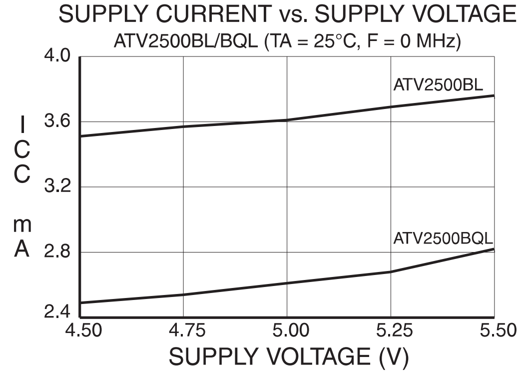
SUPPLY CURRENT vs. INPUT FREQUENCY



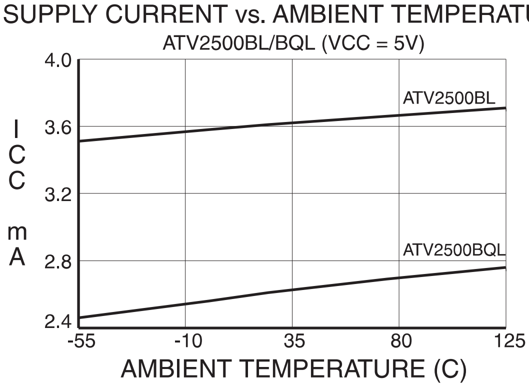
SUPPLY CURRENT vs. SUPPLY VOLTAGE



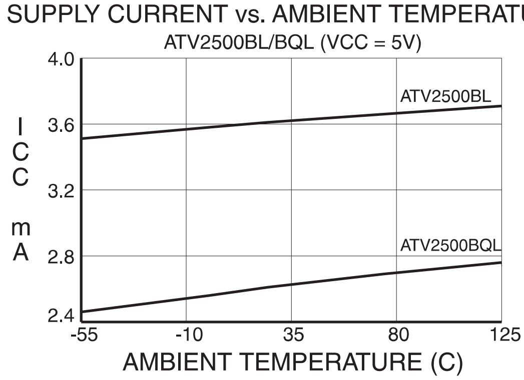
SUPPLY CURRENT vs. SUPPLY VOLTAGE



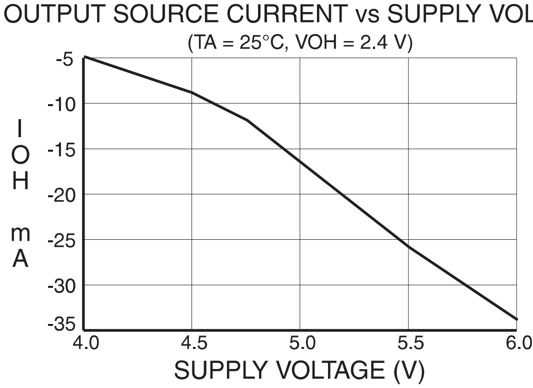
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



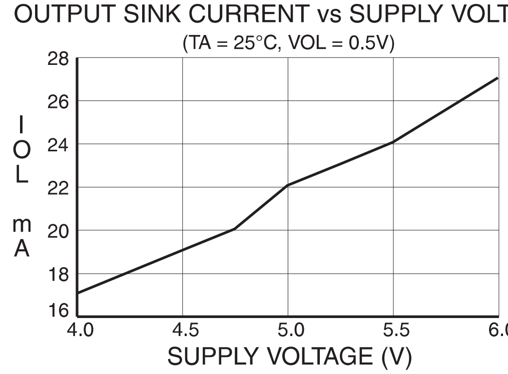
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



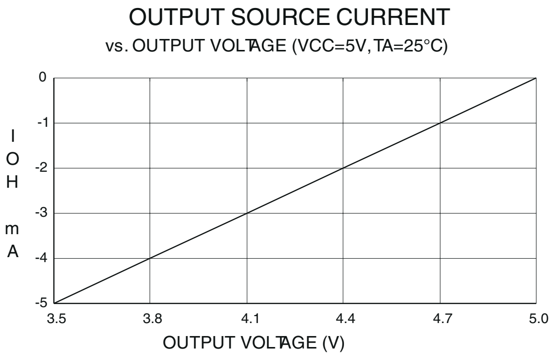
OUTPUT SOURCE CURRENT vs SUPPLY VOLTAGE

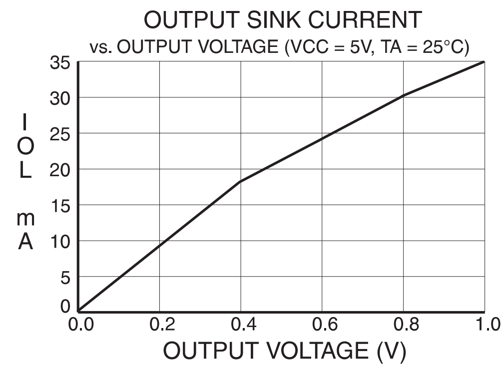


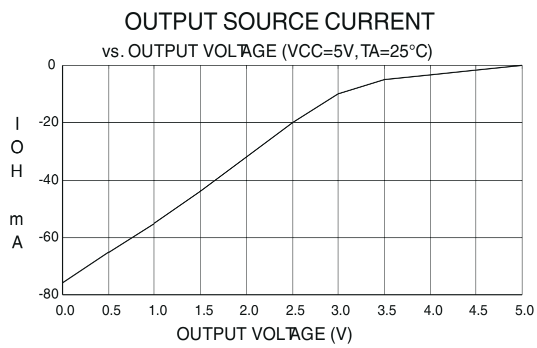
OUTPUT SINK CURRENT vs SUPPLY VOLTAGE

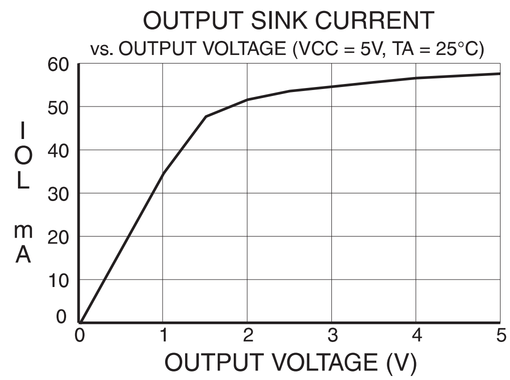


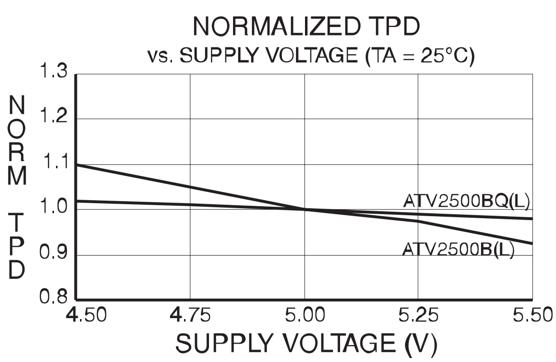
Note: 1. All normalized values referenced to maximum specification in AC Characteristics of data sheet.

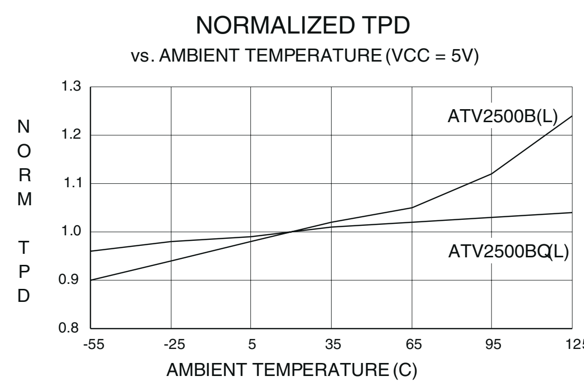


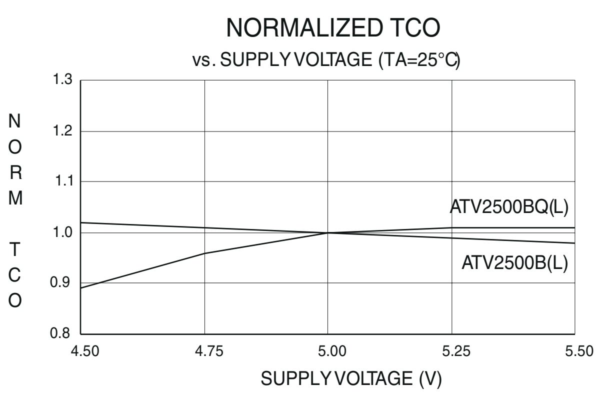


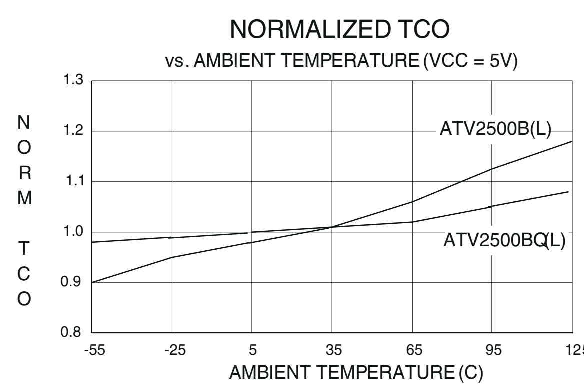




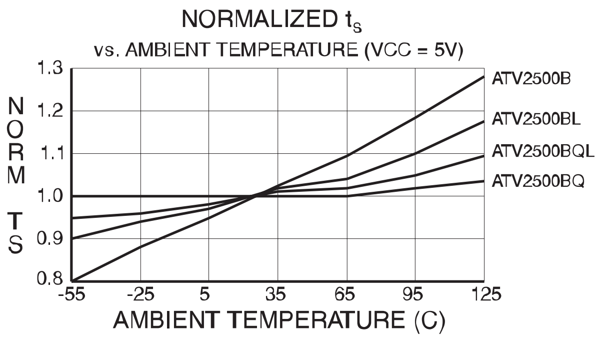


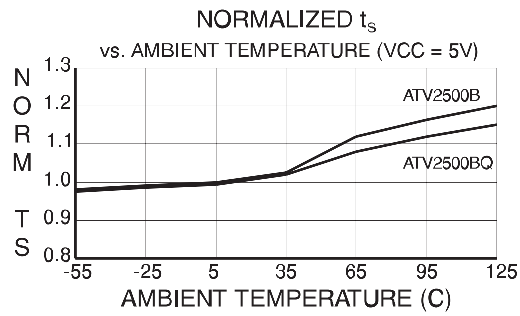


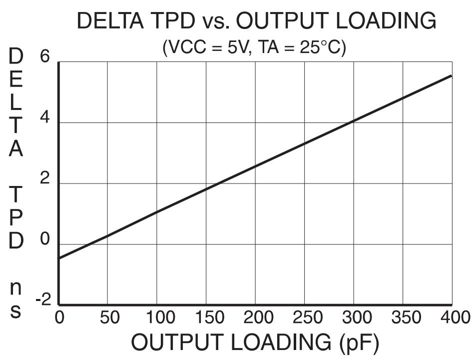


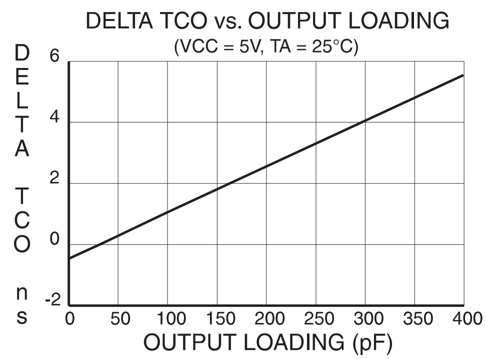


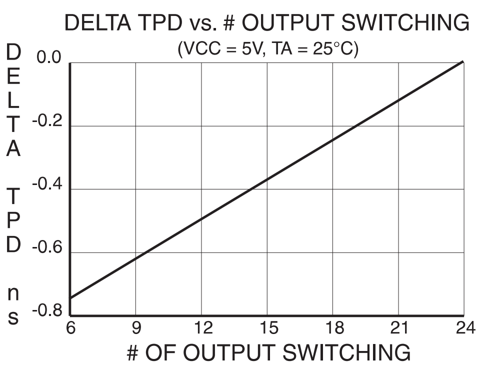
Note: 1. All normalized values referenced to maximum specification in AC Characteristics of data sheet.

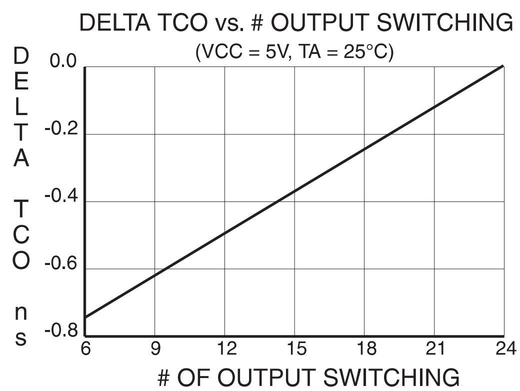


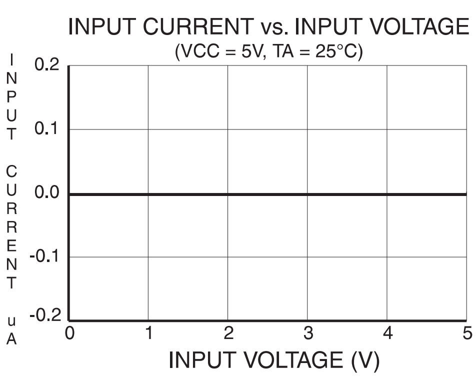


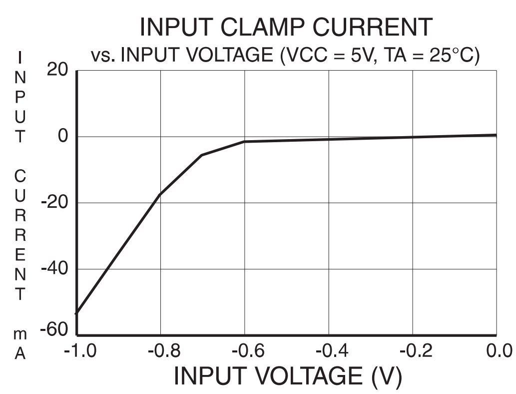












Note: 1. All normalized values referenced to maximum specification in AC Characteristics of data sheet.

Ordering Information

t_{PD} (ns)	t_{COS} (ns)	Ext. f_{MAXS} (MHz)	Ordering Code	Package	Operation Range
12	7.5	69	ATV2500B-12JC ATV2500B-12KC	44J 44KW	Commercial (0°C to 70°C)
15	10	52	ATV2500B-15JC ATV2500B-15KC	44J 44KW	Commercial (0°C to 70°C)
			ATV2500B-15JI ATV2500B-15KI	44J 44KW	Industrial (-40°C to 85°C)
			ATV2500B-15KM ATV2500B-15LM	44KW 44LW	Military (-55°C to 125°C)
			ATV2500B-15KM/883 ATV2500B-15LM/883	44KW 44LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
20	11	40	ATV2500BL-20JC ATV2500BL-20KC	44J 44KW	Commercial (0°C to 70°C)
			ATV2500BL-20JI ATV2500BL-20KI	44J 44KW	Industrial (-40°C to 85°C)
			ATV2500BL-20KM ATV2500BL-20LM	44KW 44LW	Military (-55°C to 125°C)
			ATV2500BL-20KM/883 ATV2500BL-20LM/883	44KW 44LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
20	11	40	ATV2500BQ-20DC ATV2500BQ-20JC ATV2500BQ-20KC ATV2500BQ-20PC	40DW6 44J 44KW 40P6	Commercial (0°C to 70°C)

Using “C” Product for Industrial

To use commercial product for Industrial temperature ranges, down-grade one speed grade from the “I” to the “C” device (7 ns “C” = 10 ns “I”) and de-rate power by 30%.

Package Type	
40DW6	40-pin, 0.600" Wide, Ceramic, Dual Inline Package (Cerdip)
44J	44-lead, Plastic J-leaded Chip Carrier OTP (PLCC)
44KW	44-lead, Windowed, Ceramic J-leaded Chip Carrier (JLCC)
40P6	40-pin, 0.600" Wide, Plastic, Dual Inline Package OTP (PDIP)
44LW	44-pad, Windowed, Ceramic Leadless Chip Carrier (LCC)

Ordering Information (Continued)

t_{PD} (ns)	t_{COS} (ns)	Ext. f_{MAXS} (MHz)	Ordering Code	Package	Operation Range
25	12	31	ATV2500BQ-25DC ATV2500BQ-25JC ATV2500BQ-25KC ATV2500BQ-25PC	40DW6 44J 44KW 40P6	Commercial (0°C to 70°C)
			ATV2500BQ-25DI ATV2500BQ-25JI ATV2500BQ-25KI ATV2500BQ-25PI	40DW6 44J 44KW 40P6	Industrial (-40°C to 85°C)
			ATV2500BQ-25DM ATV2500BQ-25KM ATV2500BQ-25LM	40DW6 44KW 44LW	Military/883C (-55°C to 125°C)
			ATV2500BQ-25DM/883 ATV2500BQ-25KM/883 ATV2500BQ-25LM/883	40DW6 44KW 44LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
25	12	31	ATV2500BQL-25DC ATV2500BQL-25JC ATV2500BQL-25KC ATV2500BQL-25PC	40DW6 44J 44KW 40P6	Commercial (0°C to 70°C)
25	12	31	ATV2500BQL-25DI ATV2500BQL-25JI ATV2500BQL-25KI ATV2500BQL-25PI	40DW6 44J 44KW 40P6	Industrial (-40°C to 85°C)
30	15	26	ATV2500BQL-30DM ATV2500BQL-30KM ATV2500BQL-30LM	40DW6 44KW 44LW	Military/883C (-55°C to 125°C)
	15	26	ATV2500BQL-30DM/883 ATV2500BQL-30KM/883 ATV2500BQL-30LM/883	40DW6 44KW 44LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant

Using “C” Product for Industrial

To use commercial product for Industrial temperature ranges, down-grade one speed grade from the “I” to the “C” device (7 ns “C” = 10 ns “I”) and de-rate power by 30%.

Package Type	
40DW6	40-pin, 0.600" Wide, Ceramic, Dual Inline Package (Cerdip)
44J	44-lead, Plastic J-leaded Chip Carrier OTP (PLCC)
44KW	44-lead, Windowed, Ceramic J-leaded Chip Carrier (JLCC)
40P6	40-pin, 0.600" Wide, Plastic, Dual Inline Package OTP (PDIP)
44LW	44-pad, Windowed, Ceramic Leadless Chip Carrier (LCC)

Ordering Information (Continued)

t_{PD} (ns)	t_{COS} (ns)	Ext. f_{MAXS} (MHz)	Ordering Code	Package	Operation Range
15	10	52	5962 - 9154504MXX 5962 - 9154504MYX	44LW 44KW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
20	11	40	5962 - 9154505MXX 5962 - 9154505MYX	44LW 44KW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
25	12	31	5962 - 9154506MXX 5962 - 9154506MYX 5962 - 9154506MQA	44LW 44KW 40DW6	Military/883C (-55°C to 125°C) Class B, Fully Compliant
30	15	26	5962 - 9154507MXX 5962 - 9154507MYX 5962 - 9154507MQA	44LW 44KW 40DW6	Military/883C (-55°C to 125°C) Class B, Fully Compliant

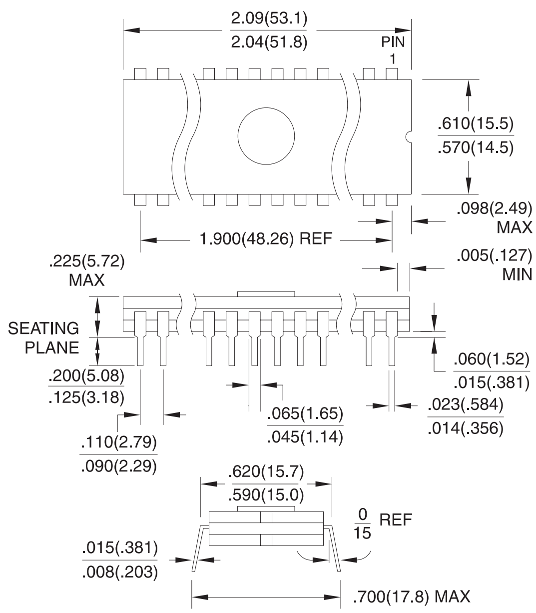
Using “C” Product for Industrial

To use commercial product for Industrial temperature ranges, down-grade one speed grade from the “I” to the “C” device (7 ns “C” = 10 ns “I”) and de-rate power by 30%.

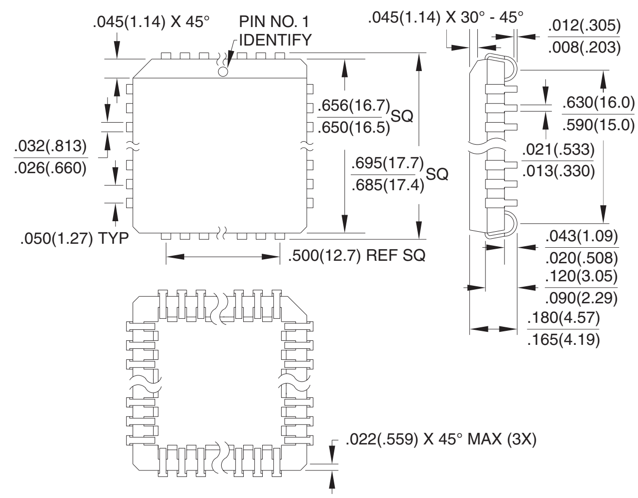
Package Type	
40DW6	40-pin, 0.600" Wide, Ceramic, Dual Inline Package (Cerdip)
44J	44-lead, Plastic J-leaded Chip Carrier OTP (PLCC)
44KW	44-lead, Windowed, Ceramic J-leaded Chip Carrier (JLCC)
40P6	40-pin, 0.600" Wide, Plastic, Dual Inline Package OTP (PDIP)
44LW	44-pad, Windowed, Ceramic Leadless Chip Carrier (LCC)

Packaging Information

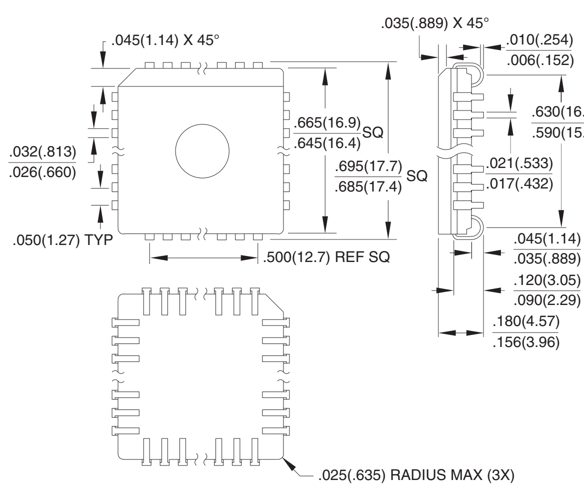
40DW6, 40-pin, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
Dimensions in Inches and (Millimeters)
MIL-STD-1835 D-5 CONFIG A



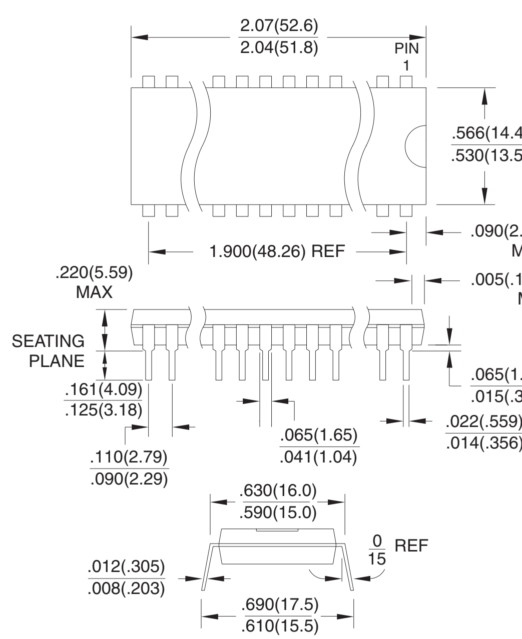
44J, 44-lead, Plastic J-leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-018 AC



44KW, 44-lead, Windowed, Ceramic J-leaded Chip Carrier (JLCC)
Dimensions in Inches and (Millimeters)
MIL-STD-1835 CJ1

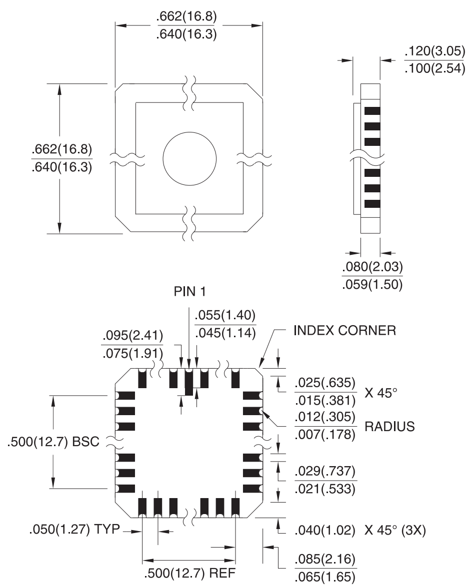


40P6, 40-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)
JEDED STANDARD MS-011 AC



Packaging Information

44LW, 44-pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
Dimensions in Inches and (Millimeters)*
MIL-STD-1835 C-5



*Controlling dimension: millimeters

Atmel Headquarters

Corporate Headquarters
2325 Orchard Parkway
San Jose, CA 95131
TEL (408) 441-0311
FAX (408) 487-2600

Europe
Atmel U.K., Ltd.
Coliseum Business Centre
Riverside Way
Camberley, Surrey GU15 3YL
England
TEL (44) 1276-686-677
FAX (44) 1276-686-697

Asia
Atmel Asia, Ltd.
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimhatsui
East Kowloon
Hong Kong
TEL (852) 2721-9778
FAX (852) 2722-1369

Japan
Atmel Japan K.K.
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
TEL (81) 3-3523-3551
FAX (81) 3-3523-7581

Atmel Operations

Atmel Colorado Springs
1150 E. Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
TEL (719) 576-3300
FAX (719) 540-1759

Atmel Rousset
Zone Industrielle
13106 Rousset Cedex
France
TEL (33) 4-4253-6000
FAX (33) 4-4253-6001

Fax-on-Demand
North America:
1-(800) 292-8635
International:
1-(408) 441-0732

e-mail
literature@atmel.com

Web Site
http://www.atmel.com

BBS
1-(408) 436-4309

Printed on recycled paper.

0249J–05/00/xM